**ملحق الجلسة السادسة ( تطبيقات مهمة):**

**تطبيق ( عداد بخانة واحدة ) :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity counter is

**Port ( seg : out STD\_LOGIC\_VECTOR (6 downto 0);**

**clk : in STD\_LOGIC ;**

**sel : out STD\_LOGIC);**

end counter;

architecture Behavioral of counter is

**signal q:integer range 0 to 50000000 ;**

**signal c:integer range 0 to 10 ;**

begin

**sel <= '0';**

**count: process(clk)**

**begin**

**if(clk'event and clk = '1')then**

**q <= q + 1;**

**if(q = 50000000)then**

**c <= c + 1;**

**if(c = 10)then c <= 0;**

**end if;**

**end if;**

**end if;**

**end process count;**

**seg <= "0000001" when c = 0**

**else "1001111" when c = 1**

**else "0010010" when c = 2**

**else "0000110" when c = 3**

**else "1001100" when c = 4**

**else "0100100" when c = 5**

**else "0100000" when c = 6**

**else "0001111" when c = 7**

**else "0000000" when c = 8**

**else "0000100" when c = 9**

**else "1111111"; -- Don't Care**

end Behavioral;

**UCF CODE:**

NET seg<0> LOC = v14 ;

NET seg<1> LOC = w16;

NET seg<2> LOC = ab21;

NET seg<3> LOC = aa21 ;

NET seg<4> LOC = aa19 ;

NET seg<5> LOC = v16 ;

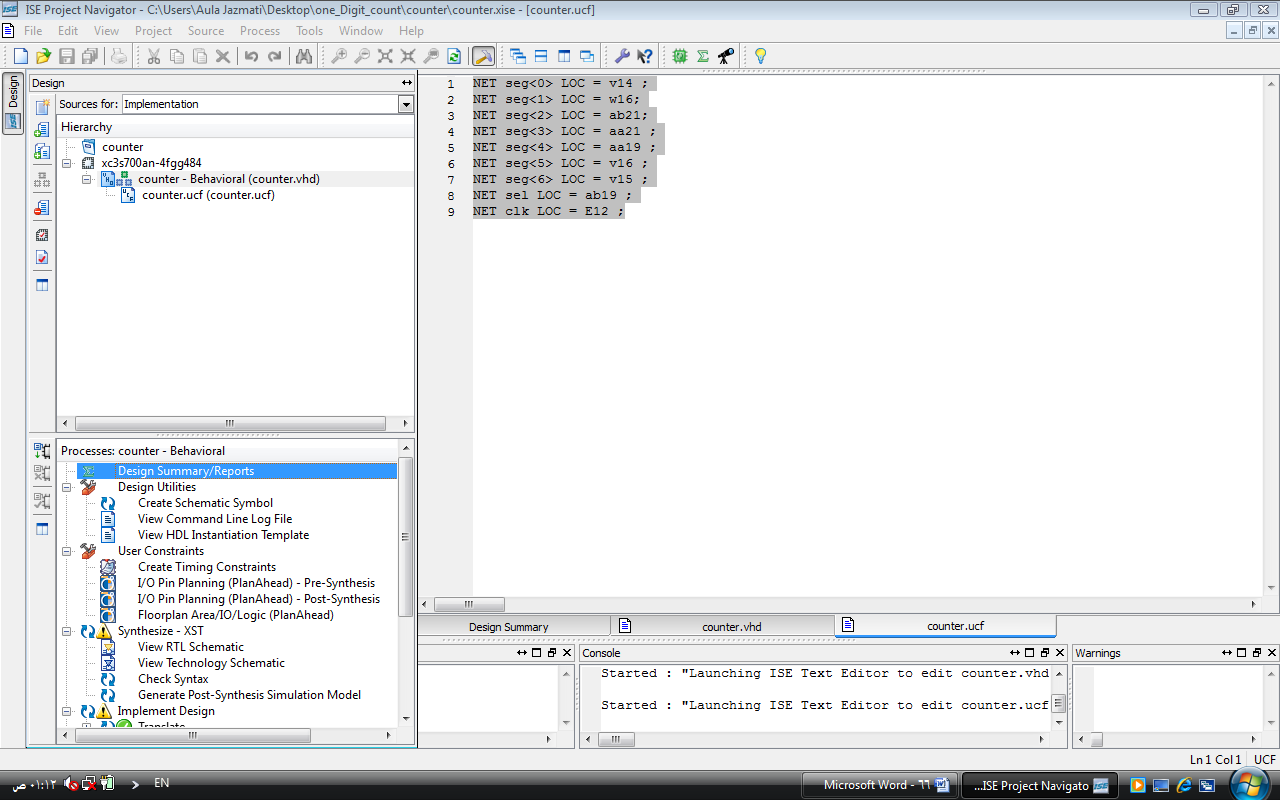
NET seg<6> LOC = v15 ;

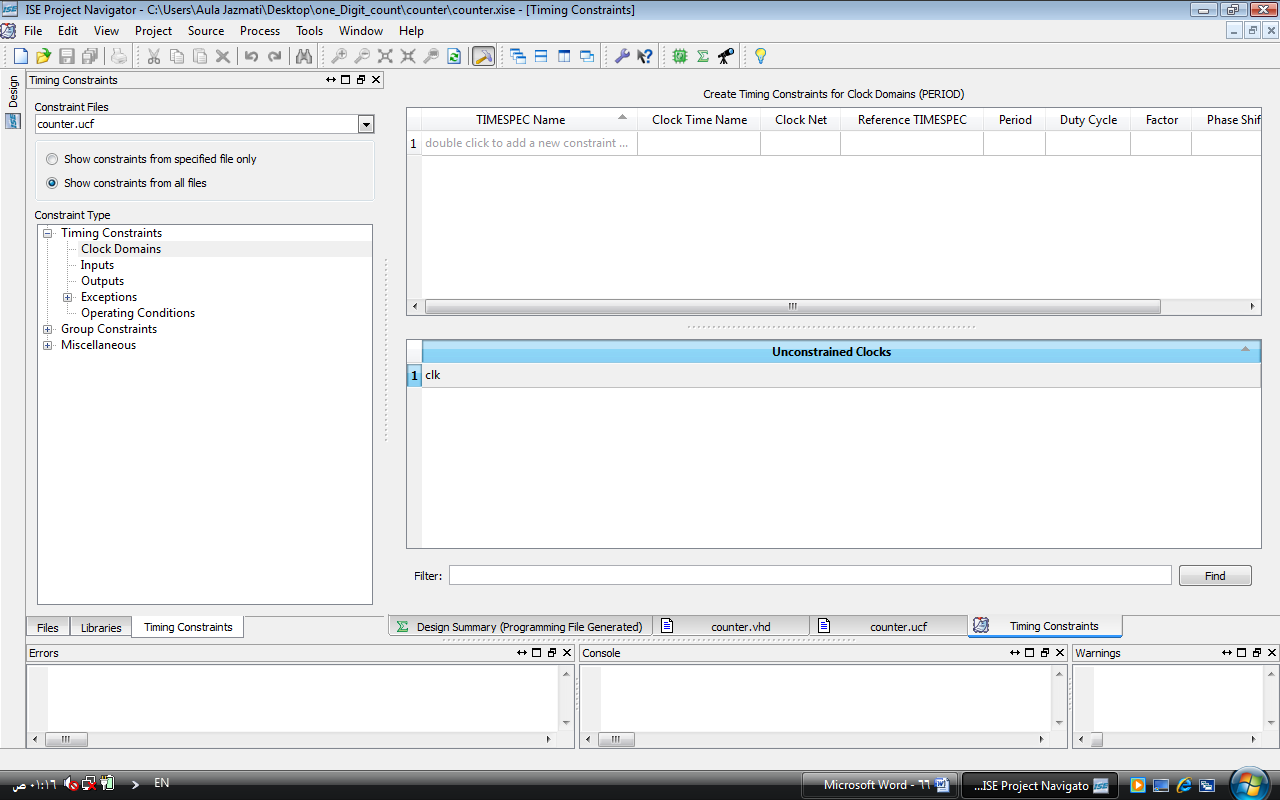
NET sel LOC = ab19 ;

**NET clk LOC = E12 ;**

**ملاحظات مهمة:**

لتنفيذ البرنامج الذي يحتوي نبضات ساعة نتبع الخطوتين التاليتين بعد انشاء ملف قيود المستخدم و قبل كتابة تعليمات الاسناد فيه.

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**Clock Sources**

The Spartan-3A/3AN Starter Kit board supports three primary clock input sources**:**

1. The board includes an on-board **50 MHz clock oscillator**.
2. Clocks can be supplied off-board via an SMA-style connector. Alternatively, the **FPGA can generate clock signals or other high-speed signals on the SMA-style connector**.
3. A **133 MHz clock oscillator** is installed in the CLK\_AUX socket. Optionally substitute , a separate eight-pin DIP-style clock oscillator in the provided socket.

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**تطبيق2 :**

في البرنامج التالي أخطاء عديدة , والمطلوب تصحيحها.

library IEEE

use IEEE.STD\_LOGIC\_1164.ALL

use IEEE.STD\_LOGIC\_ARITH.ALL

use IEEE.STD\_LOGIC\_UNSIGNED.ALL

entity D\_FF is

Port ( Q : out STD\_LOGIC

Din : in STD\_LOGIC

clk : in STD\_LOGIC

rst : in STD\_LOGIC(

architecture Behavioral of D\_FF is

begin

**D\_act :process (clk,rst)**

**begin**

**IF (rst='1') THEN**

**Q <= '0';**

**ELSIF (clk'EVENT AND clk='1') THEN Q <= Din;**

**END IF;**

end process D\_act

end Behavioral